REMARKS

The Office Action dated February 23, 2004 has been received and carefully considered. Claim 11 has been amended and claims 21 and 22 have been canceled. No new matter is introduced by the amendments to claim 11. Reconsideration of the outstanding rejections in the present application therefore is respectfully requested based on the following remarks.

Objection to Figure 2

At page 2 of the Office Action, Figure 2 was objected to for having the reference characters "106," "120" and "300" all being used to designate an SRAM cell. The replacement Figure 2 attached as Appendix A has been amended to remove the reference characters "106" and "120" so that only the reference character "300" designates the SRAM cell. Applicants therefore respectfully request entry thereof and withdrawal of this objection.

Objection to the Specification

At page 2 of the Office Action, the specification was objected to for having section headings in bold type. Applicants have amended the section headings accordingly. Entry thereof is respectfully requested.

The Examiner also appears to object to the specification for not having each of the sections headings listed in 37 C.F.R. 1.77(b) and further appears to request that the Applicants amend the specification so that each section heading is listed and if no text follows a particular section heading, to place the phrase "Not Applicable" following the section heading as the Examiner alleges is required by 37 C.F.R. 1.77(b). However, 37 C.F.R. 1.77(c) provides that "[t]he text of the specification sections defined in paragraphs (b)(1) through (b)(11) of this section, *if applicable*, should be preceded by a section heading in uppercase and without underlining or bold type" (emphasis added). Thus, there is no requirement to list each section heading and to provide the phrase "Not Applicable" if the section is not applicable. The Applicants therefore have elected to forgo amending the specification to include non-applicable section headings.

In view of the forgoing, it is respectfully submitted that the objection to the specification is improper at this time and withdrawal of this objection therefore is respectfully requested.

Anticipation Rejection of Claims 1-9, 11-19, 21 and 22

At page 3 of the Office Action, claims 1-9, 11-19, 21 and 22 were rejected under 35 U.S.C. § 102(b) as being anticipated by Matsumura (U.S. Patent No. 5,365,475). This rejection is respectfully traversed.

Claim 1, from which claims 2-10 depend, recites, in part, the limitations of a static random access memory (SRAM) device *capable of storing a program that is accessible when said SRAM device is powered up.* Claim 1 further recites the limitations of wherein the SRAM device comprises a plurality of storage cells, *each storage cell comprising a data latch comprising a biasing circuit* capable of forcing at least one of a first and second I/O lines to a known logic state when power is applied to said SRAM device, *wherein said known logic state comprises a portion of said program.* Claim 11, from which claims 12-20 depend, has been amended to recite similar limitations. The Examiner asserts that Matsumura discloses these limitations and cites col. 1, lines 15-19 and Figure 3 of Matsumura in support of this assertion. However, it is respectfully submitted that neither the cited passages nor any other passage of Matsumura disclose a SRAM device capable of storing a program accessible when the SRAM device is powered up as recited in claims 1 and 11. Instead, the passage at col. 1, lines 15-19 of Matsumura (cited by the Examiner) merely states that the invention of Matsumura relates to "a semiconductor memory device which is usable as both a static type memory and a read-only memory" and fails to mention the storage of a program accessible when the memory device is powered up.

It is also respectfully submitted that, contrary to the Examiner's assertions, Matsumura fails to disclose the limitations of each of a plurality of storage cells of the SRAM device comprising a biasing circuit capable of forcing at least one of first and second I/O lines to a known logic state when power is applied to the SRAM device, wherein the known logic state comprises a portion of the program, as recited in claims 1 and 11. Firstly, Matsumura fails to disclose the storage of a program in the SRAM devices, as noted above, and thus necessarily fails to disclose the forcing of at least one of first and second I/O lines to a known logic state

where the known logic state comprises a portion of the program. Secondly, Matsumura fails to disclose the limitations of each of the plurality of storage cells comprising a biasing circuit for forcing at least one of the first and second I/O lines to a known logic state. With respect to these limitations, the Examiner asserts that the G_1, G_2 ground lines and the V_1 and V_2 supply lines disclosed in Figure 3 of Matsumura are the equivalent of the biasing circuit recited in claims 1 and 11. *See* Office Action, p. 4. However, the Applicants respectfully submit that the G_1, G_2, V_1 and V_2 lines of Matsumura are merely a collection of lines (*see, e.g.*, Matsumura, col. 5, line 66 to col. 6, line 58) and therefore do not comprise a biasing *circuit* as understood from the context of the claims and specification of the present application. Moreover, claims 1 and 11 recite the limitations of each storage cell including its own biasing circuit, whereas Matsumura discloses the provision of the power and ground lines to each memory cell, so that the power and ground lines are common to, or shared by, all of the memory cells.

In view of the foregoing, the Applicants respectfully submit that Matsumura fails to disclose or suggest each and every limitation recited in independent claims 1 and 11. Matsumura therefore fails to disclose or suggest each and every limitation recited in claims 2-10 and 12-20 at least by virtue of their dependency from one of claims 1 and 11. Moreover, these claims recite additional features that are not disclosed or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully submitted that the anticipation rejection of claims 1-9, 11-19 and 21-22 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 10 and 20

At page 8 of the Office Action, claims 10 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumura in view of Shimazu (U.S. Patent No. 4,777,623). This rejection is respectfully traversed.

As noted above, Matsumura fails to disclose at least the limitations of a SRAM device capable of storing a program that is accessible when said SRAM device is powered up and further wherein the SRAM device comprises a plurality of storage cells, each storage cell

comprising a data latch comprising a biasing circuit capable of forcing at least one of a first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program, as presently recited in claims 1 and 11, from which claims 10 and 20 respectively depend. The Applicants respectfully submit that Shimazu also fails to disclose at least these limitations.

Moreover, the Applicants respectfully submit that, contrary to the Examiner's assertions, Shimazu fails to disclose the limitations of a biasing circuit comprising a grounding circuit selectively connected by a programmable connect to one of the first inverter output and second inverter output as recited in claims 10 and 20. As a first matter, Shimazu fails disclose a grounding circuit *selectively* connected to one of a first inverter output and a second inverter output. Instead, Shimazu discloses a grounding circuit *fixedly* connected to only one inverter's output. As a second matter, Shimazu fails to disclose a *programmable connect* for selectively connecting the grounding circuit to one of the first and second inverter outputs as presently recited in claims 10 and 20.

In view of the foregoing, it is respectfully submitted that the combination of Matsumura and Shimazu as proposed by the Examiner fails to disclose or even suggest each and every limitation of claims 10 and 20 and the obviousness rejection of claims 10 and 20 therefore is improper at this time. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

In view of the foregoing, the Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicants do not believe that any additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 01-0365.

Respectfully submitted,

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Date

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